WHAT IS CLAIMED IS:

1. A buffer amplifier architecture for buffering signals that are supplied in parallel to substantially identical chips on a semiconductor circuit module, comprising:

first receiver elements for respective parallel reception of the signals;

first output buffer amplifiers, whose input is respectively connected to an output on a respective first receiver element, for receiving signals from the first receiver elements and producing buffered output signals that are supplied to the chips on the semiconductor circuit module via a signal line network; and

first delay circuits with an adjustable delay time, Δt_{var}, which are respectively connected between the output of each first receiver element and the input of each first output buffer amplifier, and delay the signals received from the respective receiver element in accordance with a set delay time, $\Delta t_{var.}$

2. The buffer amplifier architecture of claim 1, further comprising:

a second set of receiver elements for receiving a system clock signal;

a second output buffer amplifiers, whose input is connected to an output on the second receiver element, for the purpose of producing a buffered output clock signal;

a second delay circuit with an adjustable delay time, Δt_{var}, which is provided between the output of the second receiver element and the input of the second output buffer amplifier for the purpose of delaying the output of the clock signal received from the second receiver element in accordance with the set delay time, Δt_{var}; and

a delay detector circuit having a first and a second input, where the first input is connected to the output of the second receiver element and the second input is connected via a

feedback loop to the output of the second output buffer amplifier, for the purpose of detecting an actual delay time between the clock signals applied to its first and second inputs.

3. The buffer amplifier architecture of claim 2, wherein the delay detector circuit further comprises:

a third input, to which a reference signal indicating a nominal delay is applied, and a differential amplifier arranged to produce a control voltage that corresponds to the difference between the detected actual delay time and the nominal delay time indicated by the reference signal, and which is respectively supplied to a control input on the first and second delay circuits for the purpose of setting the delay time, t_{var}.

4. The buffer amplifier architecture of claim 1, wherein the chips are DRAM chips, and wherein the semiconductor circuit module is a DRAM memory module.

5. The buffer amplifier architecture in claim 1, wherein the feedback loop includes

a reference line network having the same structure and the same electrical properties as capacitance elements that terminate the signal line network and the reference line network, wherein the capacitance elements have the same capacitances as the signal inputs on the chips on the semiconductor circuit module.

6. The buffer amplifier architecture of claim 5, wherein the capacitance elements are produced by dummy pins on the chips.

7. The buffer amplifier architecture of claim 5, wherein the capacitance elements are produced by unused signal inputs on the chips.

8. The buffer amplifier architecture of claim 1, wherein the signals buffered by the buffer amplifier architecture are command and address signals for memory chips.

9. The buffer amplifier architecture of claim 1, wherein

the first set of receiver elements and the second set of receiver elements each include differential amplifiers.

10. The buffer amplifier architecture of claim 1, wherein the first set and second set of output buffer amplifiers each include respective push-pull amplifiers.

11. The buffer amplifier architecture of claim 1, wherein the delay detector circuit further comprises:

an exclusive-OR gate connected to the first and second inputs; and

an R-C element connected to the output of the exclusive-OR gate, wherein the delay detector circuit produces a voltage level that corresponds to the actual delay time, wherein the voltage level is supplied to an inverting input of the differential amplifier in the delay detector circuit.

12. The buffer amplifier architecture of claim 9, wherein the reference signal applied to the third input is derived from the supply voltage for the exclusive-OR gate.

13. The buffer amplifier architecture in claim 1, wherein the buffer amplifier arrangement is implemented in the form of a separate integrated circuit chip.

14. The buffer amplifier architecture in claim 1, wherein the buffer amplifier architecture is integrated in another chip on the semiconductor circuit module.

15. The buffer amplifier architecture in claim 14, wherein the buffer amplifier architecture is implemented on a DRAM memory module.